

M.L.K.P.G. College, Balrampur
Online classes
Faculty of Science

1. Department name - Botany
2. Teacher name-Yugesh kumar Kasaundhan
- 3.Topic -Chemical properties of soil
 - (a)Inorganic matter of soil
 - (b)Organic matter in soil
 - (c)Colloidal properties of soil particles
4. Date- 05.05.2020
5. Time-12:15pm -1:15pm
6. Class- M.Sc.2nd semester
7. Total no.ofparticipants-17

Close Participants (17)

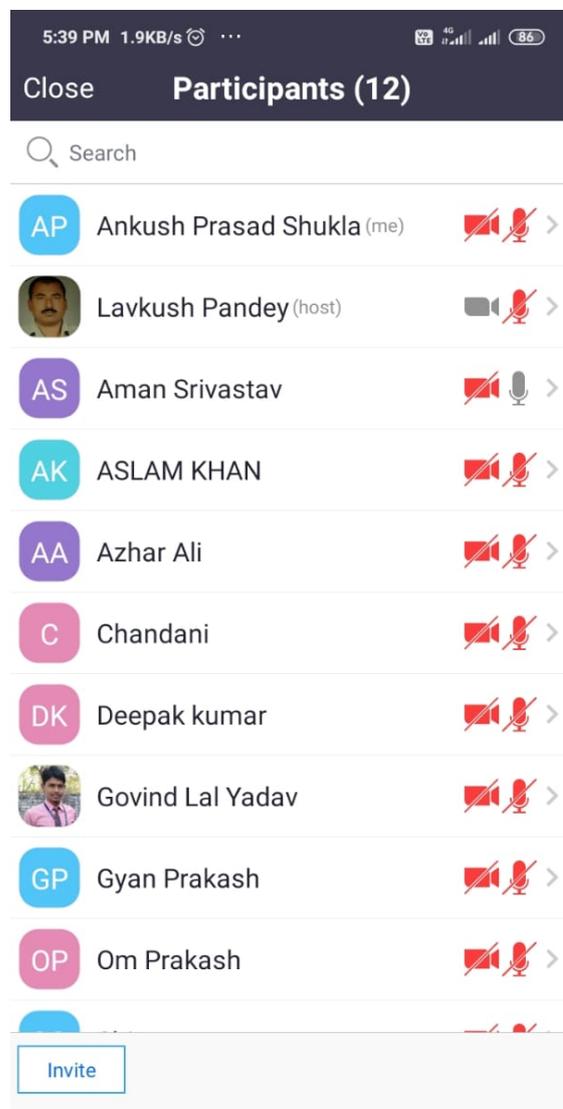
Search

Y	Yugesh Kasaundhan (me, host)	Video: Off, Audio: On
R	Nidhi Mishra	Video: Off, Audio: Off
P	Pooja Devi	Video: Off, Audio: Off
TA	TAUQEER AHMAD	Video: Off, Audio: On
V	VINOD KUMAR	Video: Off, Audio: On
GJ	Galaxy J6+	Video: Off, Audio: Off
M	Madhu pandey	Video: Off, Audio: Off
MC	Mahima Chaudhary	Video: Off, Audio: Off
P	Prabhat Pandey	Video: Off, Audio: Off

Invite Report Mute All Unmute All

M.L.K.P.G. College, Balrampur
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1. *Zoom Online Class*On 05.05.2020, 5-2:40pm
2. Department Mathematics
3. Class-M.Sc.II semester
4. Paper- V, Fluid Dynamics
5. Topic- Maximum mass flow through a nozzle, shock waves
6. Teacher- Shri Lavkush Pandey
7. 7. No of Student-12



M.L.K.P.G. College, Balrampur

Online classes

Faculty of Computer Science

- Name of teacher:** Avinash Singh
Subject Name: (Computer Architecture)
Semester: Fourth Semester
Timing: 10:00 AM to 10.45 AM
Topic: Memory Organization (Creation of RAM, difference b/w static and dynamic RAM)
No of students Present: 21
- Name of teacher:** Avinash Singh
Subject Name: Digital Electronics
Semester: Second Semester
Timing: 12.00 noon to 12.45 PM
Topic : Registers and Counters. **No of students Present:** 17

The screenshot shows a web browser displaying an NPTEL course page for 'Cache Memory'. The slide content includes:

- Cache Memory**
- locality of reference**
- temporal spatial**
- Figure 3.13:** Cache memory between CPU and the main memory

The diagram shows a CPU connected to a Cache, which is connected to Main Memory. Handwritten red annotations include 'locality of P1', 'Paging', and 'P2'. The CPU is labeled with 'Po' and 'P1', and the Main Memory is labeled with 'P2'. The Cache is labeled with 'Cache' and 'P1'. The diagram is titled 'Figure 3.13: Cache memory between CPU and the main memory'.

The screenshot shows a web browser displaying a slide titled 'Chapter 6 Registers and Counter'. The slide content includes:

- 6 Registers**
- Fig** register constructed with four D-type filpflops.
- “Clock”** triggers all flip-flops on the positive edge of each pulse.
- “Clear”** is useful for clearing the register to all 0’s prior to its

The diagram shows a 4-bit register structure with four D-type flip-flops. The inputs are labeled I_0, I_1, I_2, I_3 and the outputs are labeled A_0, A_1, A_2, A_3 . Each flip-flop has a 'D' input, a 'C' (clock) input, and an 'R' (reset) input. The clock inputs are connected to a common line, and the reset inputs are connected to a common line.

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Faculty of Computer Science

1. **Name of Teacher** : Abhishek Singh
Date & Time : 5th May, 2020, 09:00 AM to 09:30 AM
Course & Semester : B.C.A. 2nd Semester
Subject : Discrete Mathematics
Topic Covered : Graph Theory
No. of Students : 10

2. **Name of Teacher** : Abhishek Singh
Date & Time : 4th May, 2020, 04:30 PM to 05:30 PM
Course & Semester : B.C.A. 4th Semester
Subject : Networking through Linux
Topic Covered : Linux shell commands
No. of Students : 10

